



SEMIPACK® 3

Thyristor Modules

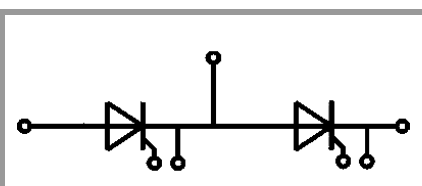
SKKT 273/18 E

Features*

- Industrial standard package
- Electrically insulated base plate
- Heat transfer through aluminum oxide ceramic insulated metal base plate
- Chip soldered on direct copper bonded Al₂O₃ ceramic
- UL recognition, file no. E63532

Typical Applications

- DC motor control (e. g. for machine tools)
- Temperature control (e. g. for ovens, chemical processes)
- Professional light dimming (studios, theaters)



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Absolute Maximum Ratings

Symbol	Conditions		Values	Unit
Chip				
$I_{T(AV)}$	sinus 180°	$T_c = 85\text{ °C}$	274	A
		$T_c = 100\text{ °C}$	204	A
I_{TSM}	10 ms	$T_j = 25\text{ °C}$	9000	A
		$T_j = 130\text{ °C}$	8000	A
i^2t	10 ms	$T_j = 25\text{ °C}$	405000	A ² s
		$T_j = 130\text{ °C}$	320000	A ² s
V_{RSM}			1900	V
V_{RRM}			1800	V
V_{DRM}			1800	V
$(di/dt)_{cr}$	$T_j = 130\text{ °C}$		130	A/μs
$(dv/dt)_{cr}$	$T_j = 130\text{ °C}$		1000	V/μs
T_j			-40 ... 130	°C
Module				
T_{stg}			-40 ... 125	°C
V_{isol}	a.c.; 50 Hz; r.m.s.	1 min	3000	V
		1 s	3600	V

Characteristics

Symbol	Conditions		min.	typ.	max.	Unit
Chip						
V _T	T _j = 25 °C, I _T = 750 A				1.6	V
V _{T(TO)}	T _j = 130 °C				0.90	V
r _T	T _j = 130 °C				0.92	mΩ
I _{DD} ;I _{RD}	T _j = 130 °C, V _{DD} = V _{DRM} ; V _{RD} = V _{RRM}				100	mA
t _{gd}	T _j = 25 °C, I _G = 1 A, di _G /dt = 1 A/μs			1		μs
t _{gr}	V _D = 0.67 * V _{DRM}			2		μs
t _q	T _j = 130 °C			150		μs
I _H	T _j = 25 °C			150	500	mA
I _L	T _j = 25 °C, R _G = 33 Ω			300	2000	mA
V _{GT}	T _j = 25 °C, d.c.		2			V
I _{GT}	T _j = 25 °C, d.c.		150			mA
V _{GD}	T _j = 130 °C, d.c.				0.25	V
I _{GD}	T _j = 130 °C, d.c.				10	mA
R _{th(j-c)}	cont.	per chip			0.104	K/W
		per module			0.052	K/W
R _{th(j-c)}	sin. 180°	per chip			0.108	K/W
		per module			0.054	K/W
R _{th(j-c)}	rec. 120°	per chip			0.122	K/W
		per module			0.061	K/W
Module						
R _{th(c-s)}	chip			0.08		K/W
	module			0.04		K/W
M _s	to heatsink M5		4.25		5.75	Nm
M _t	to terminals M8		7.65		10.35	Nm
a					5 * 9.81	m/s ²
w				410		g

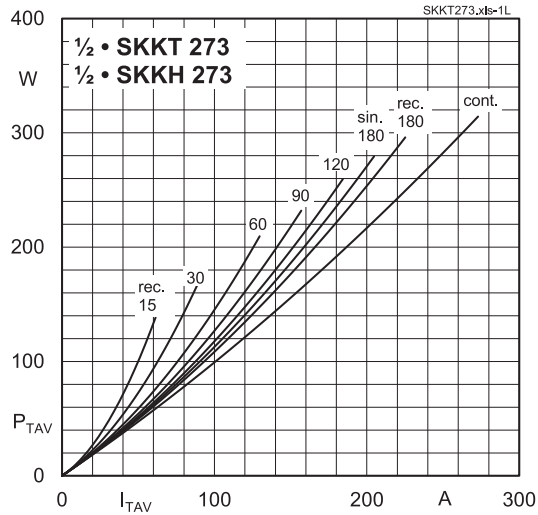


Fig. 1L: Power dissipation per thyristor/diode vs. on-state current

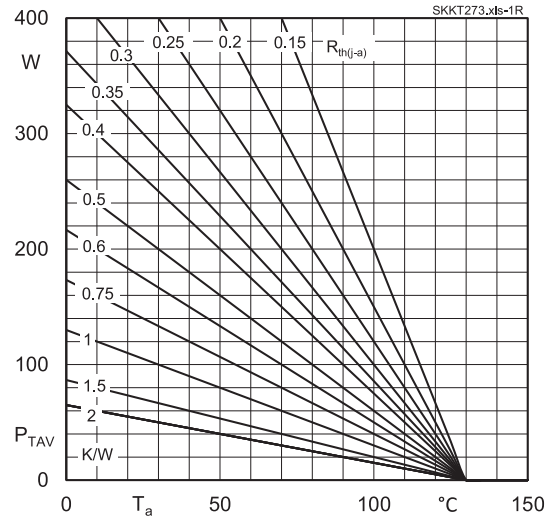


Fig. 1R: Power dissipation per thyristor/diode vs. ambient temperature

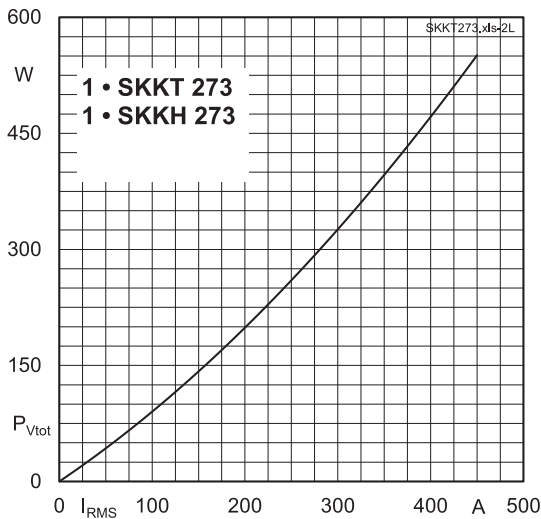


Fig. 2L: Power dissipation of one module vs. rms current

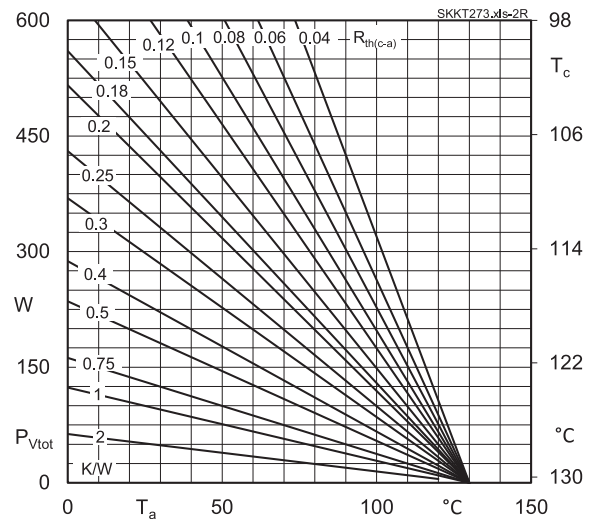


Fig. 2R: Power dissipation of one module vs. case temperature

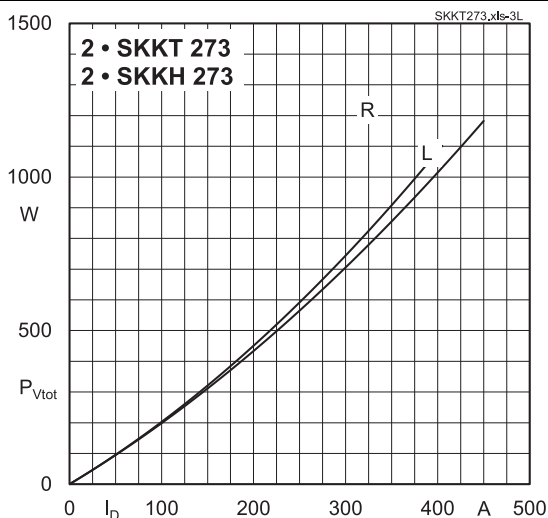


Fig. 3L: Power dissipation of two modules vs. direct current

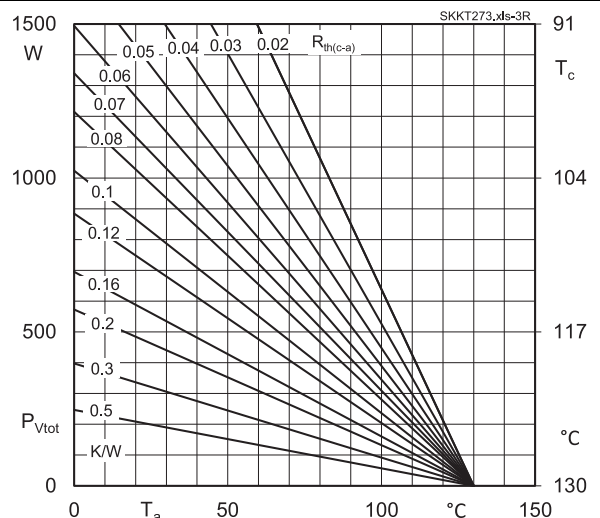


Fig. 3R: Power dissipation of two modules vs. case temperature

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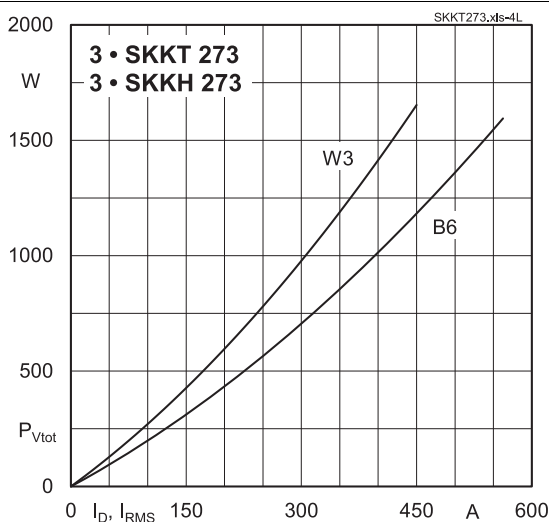


Fig. 4L: Power dissipation of three modules vs. direct and rms current

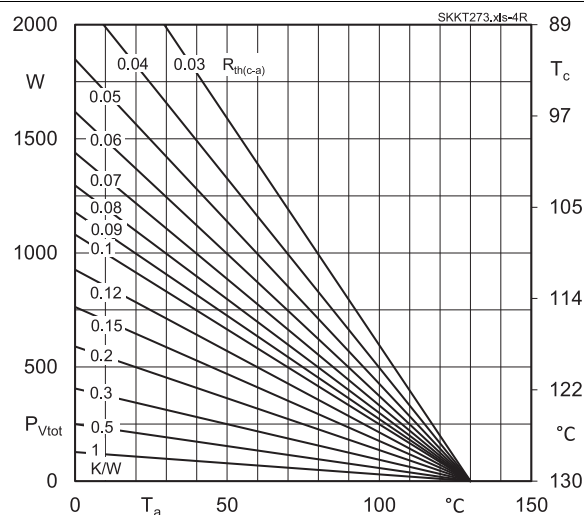


Fig. 4R: Power dissipation of three modules vs. case temperature

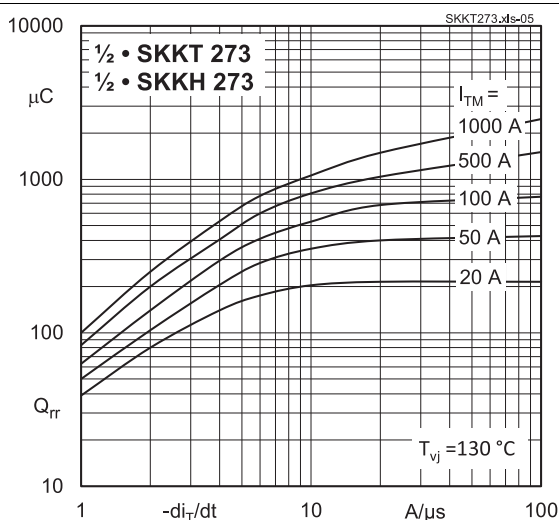


Fig. 5: Recovered charge vs. current decrease

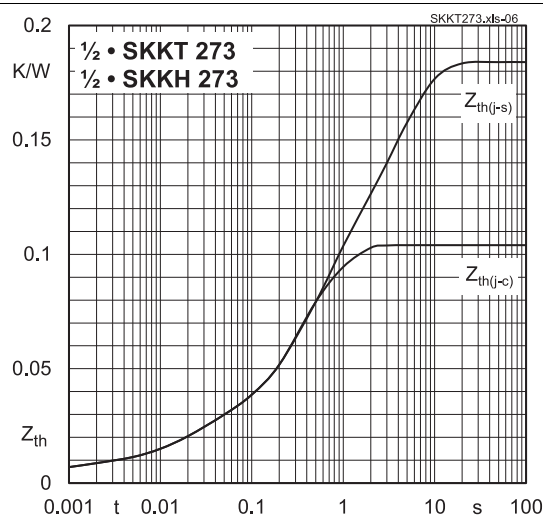


Fig. 6: Transient thermal impedance vs. time

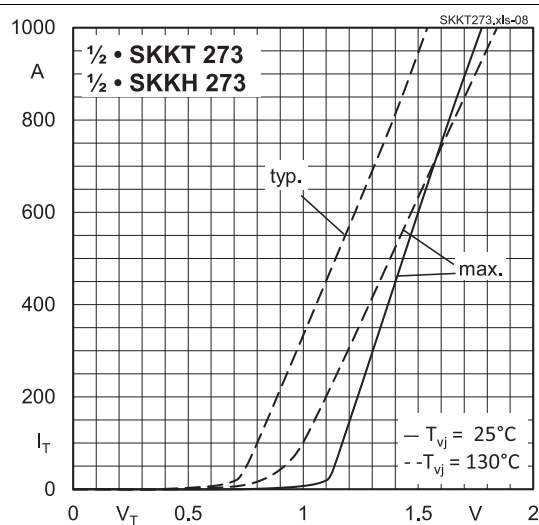


Fig. 7: On-state characteristics

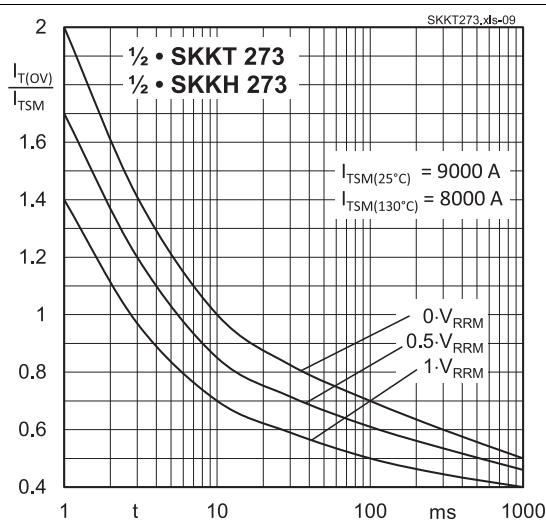


Fig. 8: Surge overload current vs. time

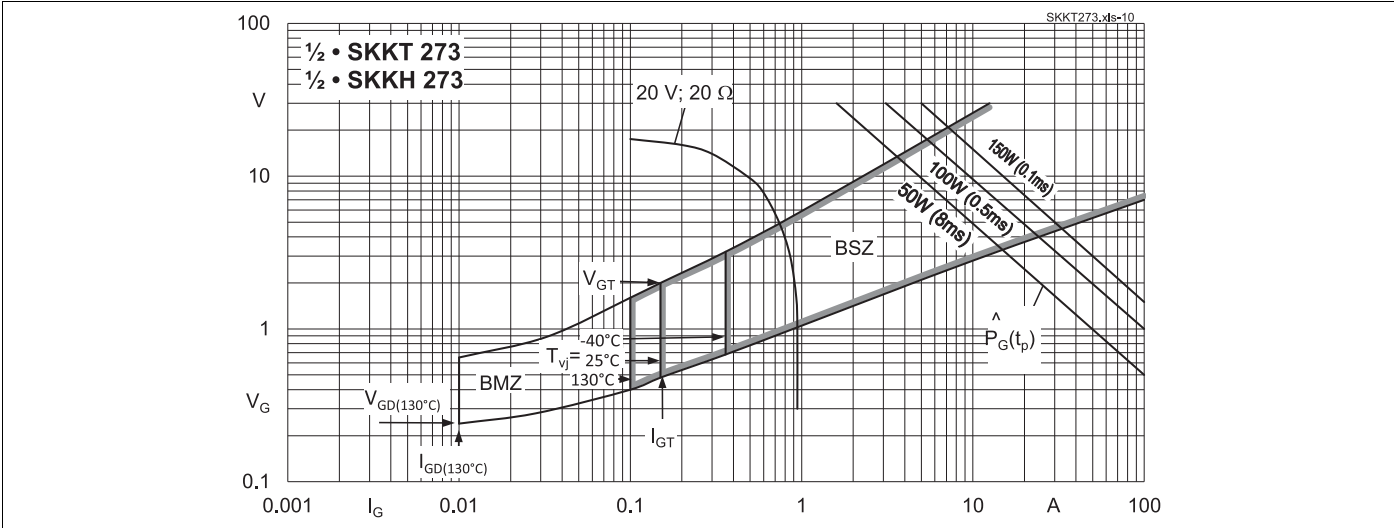
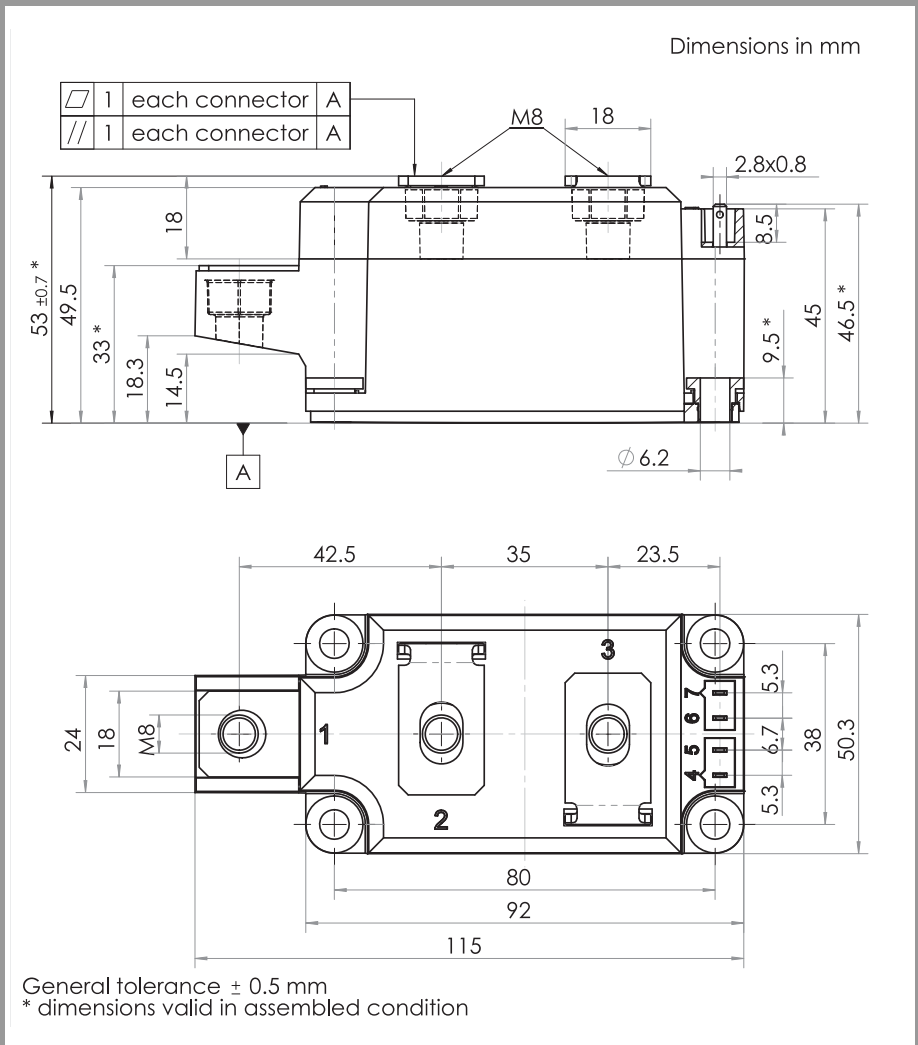


Fig. 9: Gate trigger characteristics



The diagram shows a CMOS inverter circuit. It consists of two transistors: an NMOS transistor on the left and a PMOS transistor on the right. The gates of both transistors are connected to a common input/output node labeled '1'. The NMOS transistor's source is connected to ground (labeled '6' and '7'), and its drain is connected to the PMOS transistor's source, which is also connected to ground (labeled '5' and '4'). The PMOS transistor's gate is connected to the common node '1', and its drain is connected to the output node '2'. The input node '3' is connected to the NMOS transistor's gate. The output node '2' is connected to the PMOS transistor's drain. A pull-up resistor is connected between the common node '1' and the output node '2'.

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This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, chapter IX.

*IMPORTANT INFORMATION AND WARNINGS

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